CLAIMS

What is claimed is:

1 1. A unified memory architecture that decouples a color buffer from a main memory 2 in a computer, the architecture comprising:

a memory controller connected to the main memory, the memory controller operable for partitioning an address space for the color buffer in main memory into two logical buffers, operable for designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory, operable for connecting the frame-preparation memory to a graphics subsystem and operable for connecting the refresh memory to a display device, wherein color data is written into the frame-preparation memory at a frame rate and read from the refresh memory at a rate that supports a refresh rate of the display device.

2. The unified memory architecture of claim 1, wherein the refresh memory is mapped into a dedicated memory separate from the main memory.

The unified memory architecture of claim 1, wherein the memory controller is further operable for copying the color data from the frame-preparation memory to the refresh memory.

4. The unified memory architecture of claim 3, wherein the memory controller copies the color data at pre-determined intervals.

5. The unified memory architecture of claim 3, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

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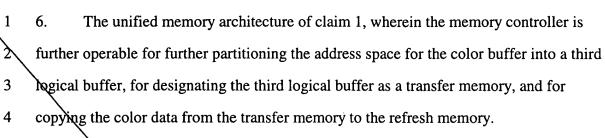
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- 7. The unified memory architecture of claim 6, wherein the memory controller is
- 2 further operable for disconnecting the logical buffer currently designated as the frame-
- 3 preparation memory from the graphics subsystem, and connecting the logical buffer
- 4 currently designated as the transfer memory to the graphics subsystem to switch the
- 5 designations of the logical buffers.

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8. The unified memory architecture of claim 7, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

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9. The unified memory architecture of claim 1, wherein the memory controller is operable for connecting the logical buffer currently designated as the frame-preparation memory to the display device and the logical buffer currently designated as the refresh memory to the graphics subsystem to switch the designations of the logical buffers.

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10. A method of decoupling a color buffer from a main memory in a computer comprising:

partitioning an address space for the color buffer in the main memory into first and second logical buffers;

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	3	•	designating the first logical buffer as a refresh memory and designating the second
	6	logical	buffer as a frame-preparation memory;
	7		writing color data into the frame-preparation memory at a frame rate;
	8	•	copying the color data from the frame-preparation memory to the refresh memory;
	\ 9	and	
	10	:	reading the color data from the refresh memory at a rate that supports a refresh
	11	rate of a	a display device.
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	1	11.	The method of claim 10, further comprising:
	2	:	mapping the refresh memory onto a dedicated memory separate from the main
<u>ال</u>	3	memory	y.
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7)\/	12.	The method of claim 10, wherein the color data is copied from the frame-
	/2	prepara	tion memory to the refresh memory when an entire frame of color data is ready for
	3	display.	
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	1	13.	The method of claim 10, wherein the color data is copied from the frame-
	2	prepara	tion memory to the refresh memory at pre-determined intervals.
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	1	14.	The method of claim 10, further comprising:
	2	:	further partitioning the address space of the color buffer into a third buffer;
	3		designating the third buffer as a transfer memory;
	4		building a first frame of color data in the frame-preparation memory;
	5	;	switching the designation of the second buffer with the designation of the third
	6	buffer v	when the first frame of color data is ready for display;
	7		building a second frame of color data in the frame-preparation memory; and

8	switching the designation of the third buffer with the designation of the second
ç	buffer when the second frame of color data is ready for display,
10	wherein copying the color data from the frame-preparation memory to the refresh
11	memory is accomplished by copying the color data from the buffer currently designated
12	2 as the transfer memory.
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1	15. A computer system comprising:
2	a processing unit;
3	a main memory connected to the processing unit though a system bus, the main
4	memory being partitioned into an address space for a color buffer;
ر ا	a memory controller connected to the main memory;
	a graphics subsystem connected to the main memory through the memory
	controller to create a frame of color data in the color buffer at a frame rate; and
	a display device connected to the main memory through the memory controller, to
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<u> </u>	wherein the memory controller decouples the color buffer from the main memory by:
	partitioning the address space for the color buffer in main memory into
일 12	two logical buffers;
[□] 13	for designating one logical buffer as a frame-preparation memory and one
14	logical buffer as a refresh memory;
15	connecting the frame-preparation memory to the graphics subsystem;
16	connecting the refresh memory to the display device; and
17	copying the color data from the frame-preparation memory to the refresh
18	B memory.

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16. The computer system of claim 15, further comprising a dedicated memory separate from the main memory and the memory controller further maps the refresh memory to the dedicated memory.

The computer system of claim 15, wherein the memory controller copies the color data at pre-determined intervals.

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18. The computer system of claim 15, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

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The computer system of claim 15, wherein the memory controller further 19. partitions the address space for the color buffer into a third logical buffer, designates the third logical buffer as a transfer memory and copies the color data from the transfer memory to the refresh memory in lieu of copying the color data from the framepreparation memory.

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20. The computer system of claim 19, wherein the memory controller further switches the designations of the logical buffers by connecting the logical buffer currently designated as the frame-preparation memory to the display system and by connecting the logical buffer currently designated as the transfer memory to the graphics subsystem.

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21. The unified memory architecture of claim 7, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

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